凌陽科技
SUNPLUS

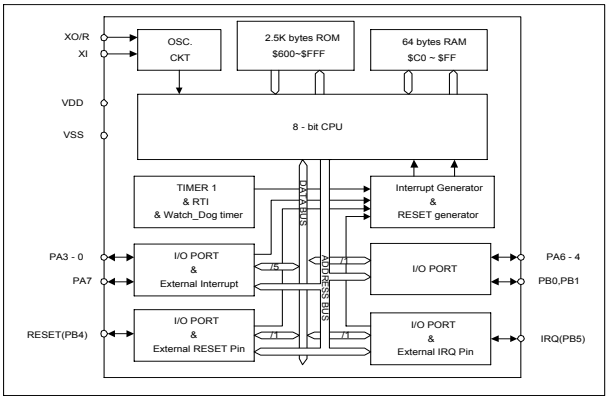
SPMC01A

MICROCONTROLLER

GENERAL DESCRIPTION

SUNPLUS SPMC01A contains a SUNPLUS 8 bit Micro-Controller Units (MCU), 12 programmable general I/Os, 2.5K bytes ROM, 64 bytes RAM and an 8-bit Timer. The advanced sub-micron CMOS process technology ensures SPMC01A's high performance, high reliability and sophisticated functionalities. In addition, SPMC01A also provides high sink current with slow output transition port pins, multi external interrupt pins, Low Voltage Reset (LVR) function, and multi oscillator options. SPMC01A offers one of the best cost/performance ratios in the industry.

BLOCK DIAGRAM



FEATURES

- Built-in 8-bit SUNPLUS CPU core and up to 6.0MHz clock operation
- 64 Bytes SRAM
- 2.5K Bytes ROM for users' program
- On-chip RC oscillator (only one external resistor needed) or crystal input or external clock input
- Total 10 programmable I/Os
- Up to 6 external interrupt pins
- 1 I/O can be with RESET input selected by Mask Option
- 3 I/Os with Slow output transition Function
- One 8-bit timer with Real Time Interrupt
- One Watchdog timer
- Power-saving STOP & WAIT modes
- Illegal address reset
- Low voltage reset circuit
- Operating Voltage Range: 2.4V - 5.5V
- Provides Chip Form, Package in PDIP or SOIC.

CPU

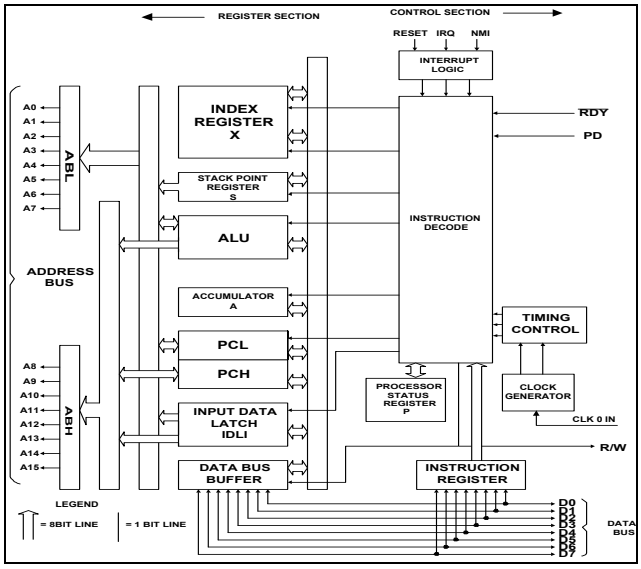
The microprocessor of SPMC01A is a SUNPLUS high performance processor equipped with Accumulator, Program Counter, X Register, Stack Pointer and Processor Status Register (The same as 6502 instruction's structure). SPMC01A is a fully static CMOS design. The oscillation frequency could be varied up to 6.0MHz depends on the application needs. The SPMC01A development system includes a SUNPLUS ICE, Evaluation Chip and Engineering Development Board.

1. PROCESSOR STATUS REGISTER

Bit	7	6	5	4	3	2	1	0
Flag	N	V	-	B	-	I	Z	C

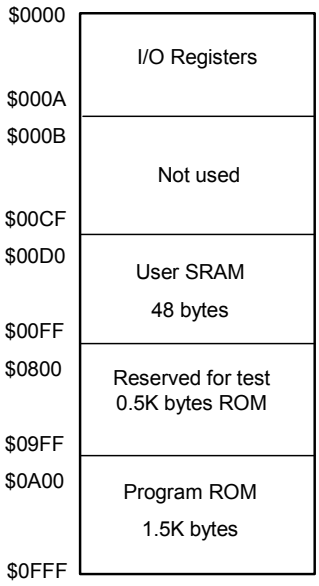
N: Negative, V: Overflow, B: Brk command, I: IRQ disable, Z: Zero, C: Carry

2. BLOCK DIAGRAM OF SUNPLUS CPU



MEMORY

1. MEMORY MAP



2. RAM

Total of sixty-four bytes of RAM (including the stack) is available from $00C0 to $00FF. The stack begins at address $00FF and proceeds down to $00C0.

3. ROM

Total of 3072 bytes of on-chip ROM including 2560 bytes of user ROM located from $0600 through $0FFF and 512 bytes of internal test ROM located from $0400 through $05FF. Users' program can only be allocated $0600 through $0FFF (2.5K).

4. NMI, RESET, IRQ VECTORS

The address of NMI (not provided in this chip), RESET and IRQ are located from $0FFA to $0FFF. The interrupt vectors should be specified in the program as follows:

```
ORG     $0FFA           ;define SPMC01A chip
                        ;interrupt vector.
DW      NMI_ROUTINE
DW      RESET
DW      INT_ROUTINE
```

When using Evaluation board with EPROM (for 27C256), the address of $7FFA must be defined as follows:

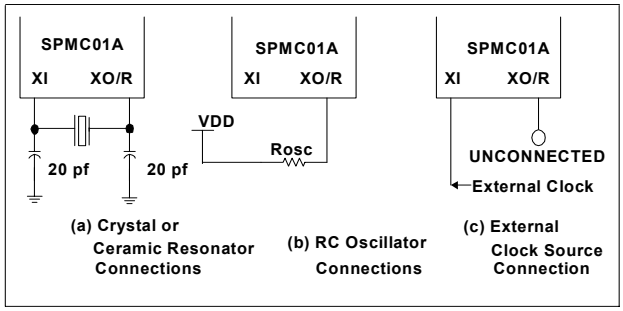
```
ORG   $7FFA              ;interrupt vector for
                         ;EPROM with
DW    NMI_ROUTINE        ;Evaluation Board.
DW    RESET
DW    INT_ROUTINE
```

When using Evaluation board with Sunplus ICE, users fill the **ORG** address of $0FFFA as follows:

```
ORG   $0FFFA             ;interrupt vector for
                         ;SUNPLUS ICE.
DW    NMI_ROUTINE
DW    RESET
DW    INT_ROUTINE
```

OSCILLATOR

The SPMC01A supports AT-cut parallel resonant oscillated Crystal /Resonator or RC oscillator or external clock sources by mask option (select one from those three types). The design of application circuit should follow the vendors' specifications or recommendations. The diagrams listed below are typical X'TAL/ROSC circuits for most applications:



MASK OPTIONS

The SPMC01A has the following mask options:

1). Oscillator Select: Crystal / Resonator or External Resistor or External Clock input.
2). PA5 - 0, PB0 Pull-down and PB1 Pull-up resistor: always disable or controllable by user's program.
3). PA3 - 0 external Interrupt capability: Enable or Disable.
4). External Interrupt Trigger (PA3 - 0 and IRQ): Edge Trigger or Edge-Level Trigger.
5). RESET / PB4 pin: I/O or I/O with RESET input function.
6). Timer clock source: fCPU/4 or fCPU/1.
7). Watch-Dog Timer Reset: Enable or Disable.
8). Low Voltage Reset: Reset on Vcc while lower than 2.2V voltage or No detection.

FUNCTION CONTROL REGISTER

All function registers will set to '0' when a reset occurred except the RT1 and RT0 will set to '1' when a reset occurred.

ADDR	REGISTER	R/W	7	6	5	4	3	2	1	0	ENABLE
$0000	PORT A DATA	R	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	
PA		W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	
$0001	PORT B DATA	R			PB5	PB4		X(0)	PB1	PB0	
PB		W			(0)	(0)		PB2	(0)	(0)	
$0002	PORT A DATA	R	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	0 = IN
DPA	DIRECTION	W	DPA7	DPA6	DPA5	DPA4	DPA3	DPA2	DPA1	DPA0	1 = OUT
$0003	PORT B DATA	R	(0)		(0)	(0)		(0)	(0)	(0)	0 = IN
DPB	DIRECTION	W	SLE		DPB5	DPB4		DPB2	DPB1	DPB0	1 = OUT
$0004	TIMER CONTROL	R	TOF(0)	RTIF(0)	TOFE	RTIE	0(0)	0(0)	RT1	RT0	
TCS	& STATUS	W			(0)	(0)	TOFR	RTIFR	(1)	(1)	1 = SET
$0005	TIMER COUNTER	R	TMR7(0)	TMR6(0)	TMR5(0)	TMR4(0)	TMR3(0)	TMR2(0)	TMR1(0)	TMR0(0)	
TCR	REGISTER	W									
$0006	IRQ CONTROL &	R	(0)	(0)			IRQF(0)	IRQF1(0)	IRQE1	IRQE	
IRQS	STATUS	W	IRQR1	IRQR					(0)	(0)	1 = SET
$0007	WATCH DOG	R									
WDT	TIMER STATUS	W								WDT(0)	1 = CLR
$0008	STOP & WAIT	R									
SNW		W				STOP(0)				WAIT(0)	1 = SET
$0009	PORTA PULLUP /	R			(0)	(0)	(0)	(0)	(0)	(0)	
RPA	DOWN REGISTER.	W			RPA5	RPA4	RPA3	RPA2	RPA1	RPA0	0 = EN
$000A	PORTB PULLUP /	R				(0)			(0)	(0)	
RPB	DOWN REGISTER.	W				RPB4			RPB1	RPB0	0 = EN

The value of bracket is power-on default value.

The gray block Is reserved.

I/O AND CONTROL REGISTER
- see Appendix A, B, C, D, F (I/O Diagram)

Total of 12 I/Os (grouped into two I/O ports, PA and PB) are provided. The descriptions are as follows:

1). The PortA (PA7 - 0) and PortB (PB1 - 0) are normal I/O ports. PA5 - 0 and PB0 have programmable pull-down. PA7 - 6 are normal I/Os and pull-up always. PB1 is normal I/O with programmable pull-up.

2). The other 2 I/Os can be used as RESET or PB4 by MASK Option and IRQ or PB5 by programming control.

1. PORT A (PA7 - 0) DESCRIPTION: (see Appendix A, B)

ADDR	REGISTER		7	6	5	4	3	2	1	0
$0000	PORT A DATA		DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
$0002	DIRECTION	0	In	In	In	In	In	In	In	In
		1	Out	Out	Out	Out	Out	Out	Out	Out
$0009	Pull-Up/Down	0	Always	Always	Pull-Down	Pull-Down	Pull-Down	Pull-Down	Pull-Down	Pull-Down
		1	Pull-Up	Pull-Up	Disable	Disable	Disable	Disable	Disable	Disable
	Up/Down resistor		5KΩ	5KΩ	100KΩ	100KΩ	100KΩ	100KΩ	100KΩ	100KΩ
	Source/sink current		-/8mA	-/8mA	-8/8mA	-8/8mA	-8/8mA	-8/8mA	-8/8mA	-8/8mA
	Special Function		Ext. INT	-	-	-	Ext. INT	Ext. INT	Ext. INT	Ext. INT

2. PORT A DATA REGISTRAR ($0000 PA)

PortA's output data will be determined by $0000 (PA Data Register) when PortA programmed as output. Any read of the PortA Data Register will return the logical state of the I/O pin when PortA is programmed as input. The PA Data Register is set to '0' when a RESET occurred.

3. PORT A DATA DIRECTION REGISTER ($0002 DPA)

The Port A can be programmed as input or output by $0002 DPA Register. When DPA = '1', the corresponding pin programmed as output. When DPA = '0', the corresponding pin programmed as input. The DPA is set to '0' (input) when a RESET occurred.

4. PORT A PULL-DOWN CONTROL REGISTER ($0009 RPA)

PA5-0 Pull-down resistors can always be disabled or controlled by user's program through mask option, but PA6 and PA7 are pull-up always. The register, RPA, is used to enable or disable the pull-up/down resistors on PA5-0, when the resistors are existing selected by mask option. **When RPA = '0'**, it will **enable** pull-down resistor of corresponding pins (PA5 - 0) at Input mode. **When RPA = '1'**, it will **disable** pull-down resistor of corresponding pins (PA5 - 0) at Input mode. No pull-down resistor is available during output mode. The RPA will be set to **'0'** (enabling mode) by RESET.

Note: SPMC01A: PA [0..5] can be pull-down or disable.

→ In SPMC05A, both pull-up and pull-down are available. However, when using SPMC05A to simulate SPMC01A and disable Rp, SUNPLUS recommends to disable Rp by setting $0009 RPA = 1 in SPMC05A.

5. PORT B (PB0, PB1, RESET/PB4, IRQ/PB5): (see Appendix A, C, D, F)

ADDR	REGISTER		7	6	5	4	3	2	1	0
$0001	PORT B DATA				IRQ/DATA	RESET/DATA		X	DATA	DATA
$0003	DIRECTION	0	SLE*		In	In		X	In	In
		1			Out	Out		Aux	Out	Out
$000A	Pull-Up/Down	0				Pull-Up			Pull-Up	Pull-Down
		1				Disable			Disable	Disable
	Up/Down resistor					100KΩ			100KΩ	100KΩ
	Source/sink current				-/8mA	-8/8mA		-/25mA	-/25mA	-8/8mA
	Special Function				IRQ	RESET			-	-

Note*: This bit is defined as SLE bit. Please refer to SLOW TRANSITION ENABLE for more detail.

6. PORT B DATA REGISTER ($0001 PB)

PortB's output data will be determined by $0001 PB Data Register when PortB is programmed as output. Any read of the PortB Data Register will return to logical state of I/O pin when PortB is programmed as input. Data register will be set to '0' when RESET occurred.

7. PORT B DATA DIRECTION REGISTER ($0003 DPB)

PortB can be programmed as input or output by $0003 DPB Register. When DPB = '1', the corresponding pin(s) is (are) programmed as output. When DPB = '0', the corresponding pin(s) is (are) programmed as input. The DPB will be set to '0' (input mode) when a RESET occurred. The direction of PB1 and PB2 must be identical.

8. PORT B PULL-UP/DOWN CONTROL REGISTER ($000A RPB)

PB0 Pull-down with PB1 Pull-up resistors can be disabled or controlled by user's program through mask option. PB4 Pull-up resistor can be disabled or controlled by user's program. The register, RPB, is used to enable or disable the pull-up/down resistors on PB0, PB1 and PB4. When RPB = '0', it will enable pull-down resistor of PB0 or pull-up of PB1, PB4 at Input mode. When RPB = '1', it will disable the corresponding pull-down resistors of PB0 or pull-up of PB1, PB4 at Input mode. No pull-down resistor is available during output mode. The RPB will be set to '0' (enabling mode) by RESET.

Note: Pull-up or down varied on different bodies
SPMC01A: PB0: Pull-down or disable, PB1: pull-up or disable
SPMC05A: PB0: Pull-down or up, PB1: No option (always pull-up)

In SPMC05A, both pull-up and pull-down are available. However, when using SPMC05A to simulate SPMC01A and disable Rp, SUNPLUS recommends to disable Rp by setting $000A RPB = 1 in SPMC05A.

9. RESET / PB4: (see Appendix D)

The RESET/PB4 pin can be selected as I/O or I/O with RESET by Mask option. When RESET is selected, RESET pin is the only external source of reset. This pin is connected to a Schmitt trigger input gate, pull-up 100KΩ (by setting $000A b4 = 0) & low active. PB4 pin is a normal I/O with programmable pull-up 100KΩ when I/O function is selected.

10. IRQ / PB5: (see Appendix F)

The IRQ/PB5 pin can be selected as I/O or I/O with IRQ by program.

1). When IRQ function is selected, the IRQ pin is the main external source of an interrupt with active-low polarity. This pin is connected to a Schmitt trigger input. It is an open-drain mode and therefore, it needs to be pulled-up externally.
2). When I/O function is selected, PB5 pin is normal I/O with open-drain always.

11. HIGH SINK CURRENT PORT: (see Appendix C)

The PB1 output current can sink 25mA or 50mA determined by the programming of DPB B1, B2, and PB B1, B2. To configure I/O mode on PB1 properly, the direction of DPB1 and DPB2 must be identical. Output sinks current as following (DPB B1 = 1 and DPB B2 = 1):

■ **The sink current is 25mA when PB B1 = 0 and PB B2 = 1.**

Example: PB0 set as input. PB1, PB4 as output.

```
LDA  #%XXX1X110      ;X don't care
STA  DPB             ;set PB4, PB1 as output, PB0
                     ;as input
LDA  #%XXX1XX00
STA  RPB             ;set PB0 pull-down, PB1
                     ;pull-up, PB4 no pull-up.
LDA  #%XXX1X10X
STA  PB              ;PB4 is "high", PB1 is "low"
                     ;& sink current is 25mA.
LDA  PB              ;from PB0 read out side
                     ;data.
AND  #%00000001      ; only used PB0
```

■ **The sink current is 50mA when PB B1 = 0 and PB B2 = 0.**

Example: PB0 set as input. PB1, PB4 as output.

```
LDA  #%XXX1X110      ;X don't care
STA  DPB             ; set PB4, PB1 as output, PB0
                     ;as input
LDA  #%XXX1XX00
STA  RPB             ;set PB0 pull-down, PB1
                     ;pull-up, PB4 no pull-up.
LDA  #%XXX1X00X
STA  PB              ;PB4 is "high", PB1 is "low"
                     ;& sink current is 50mA.
```

■ **PB1 is used as input when DPB B1 = 0 and DPB B2 = 0.**

Example: PB0, PB1, and PB4 set as input.

```
LDA  #%XXX0X000      ;X don't care
STA  DPB             ;set PB4, PB1, and PB0 as
                     ;input
LDA  #%XXX1XX00
STA  RPB             ;set PB0 pull-down, PB1
                     ;pull-up, PB4 no pull-up.
LDA  PB              ;from PB4, PB1, and PB0 read
                     ;out side data.
AND  #%00010011      ;use PB4, PB1, and PB0
```

12. EXTERNAL INTERRUPT INPUT PORTS: (see Appendix A, B, F, G)

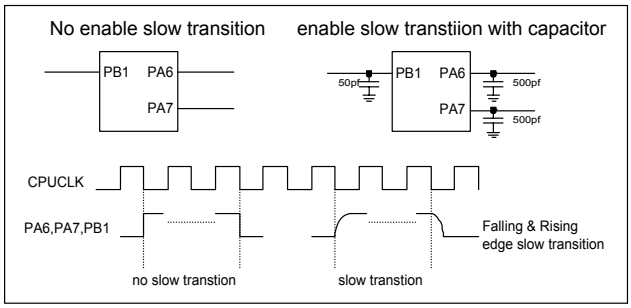
The PA3 - 0, PA7, and PB5 can be used as I/O or I/O with interrupt function. For interrupt function, PA3 - 0 interrupt is enabled or disabled by mask option and controlled by IRQE ($0006). PA7 is enabled or disabled by IRQE1 ($0006). PB5 is enabled or disabled by IRQE ($0006). For more details on interrupt statements, please see *INTERRUPT* section.

13. SLOW TRANSITION ENABLE (SLE)- $0003 bit 7 (see Appendix C)

PA6, PA7 and PB1 pins have Slow Transition signal output function (SLE). If this function is enabled ($0003 bit7 = 1), the transition time of outputs is 250ns ± 20% with 50pf(PB), 500pf(PA) loaded at 2.0MHz. When SLE ($0003 bit7) = 0, slow transition output is disabled. Note that the SLE register of SPMC01A is in $03 PORTB DATA DIRECTION. However, the SLE register of SPMC02A and SPMC05A is in $09 PORTA PULL-UP/DOWN REGISTER. If SPMC05A is used to simulate SPMC01A, the SLE should be modified for the difference before code releasing for SPMC01A.

Example: PA6, PA7 & PB1 set as output and have slow transition function.

```
        LDA   #%11XXXXXX  ;X: user-define
        STA   DPA         ;DPA $0002 port A direction,
                          ;set PA6, 7 as output
        LDA   #%1XXXX11X  ;DPB $0003 port B direction,
                          ;set PB1 as output
        STA   DPB         ;and set SLE as "1" for
                          ;enable slow transition.
        LDA   #FFh
        STA   TEMP        ; TEMP a register of $C0h~Ffh
Loop1:  LDA    TEMP
        EOR   #C2h        ;cross-change B6, B7 & B1
        STA   TEMP
        STA   PA          ;PA6, PA7 output pulse.
        STA   PB          ;PB1 output pulse
        LDX   #00h        ;delay
Loop2:  DEX
        BNE   Loop2
        JMP   Loop1       ;repeat output of PA6, PA7,
                          ;PB1.
```



RESET - see Appendix E (Reset Block Diagram)

1. EXTERNAL RESET (RESET pin) (see Appendix D, E)

The RESET/PB4 pin can be select to PB4 I/O or I/O with RESET function by Mask option. When RESET is selected, the RESET pin is the only external reset source with active-low polarity. This pin is connected to a Schmidt trigger input. It has pull-up resistor by programmed control. It is recommended to set RPB b4 as '0' to enable pull-up resistor when RESET function is applied, such does not need an external resistor.

2. POWER ON RESET (see Appendix E)

This reset is an internal reset. The Power-on-Reset will generate the reset signal that will reset the CPU until oscillator stabilized. To confirm the Power on Reset is generated properly, the system power should be held at a zero potential with respect to ground. Improper initial setting of the power might cause the system can not work properly. The CPU will become active after 4096 clock cycles.

3. WATCH DOG TIMER RESET ($0007 bit0 WDT) (see Appendix E, H)

The Watch-Dog Timer can be disabled or enabled through mask option. The internal reset of Watch-Dog will be generated by a time-out of the Watch-Dog Timer automatically when Watch-Dog is enabled. It is implemented on this device by using the output of the RTI circuit and further dividing it by eight (RT1, RT0 timing times 8). This time out generates reset if the WDT register is not clear. An internal reset is generated and reset vector is fetched. Preventing a WDT time-out reset is done by writing a '1' to WDT ($0007 b0) within a specific time. The min. WDT reset times listed in (RT1, RT0) & WDT Interrupt Frequency Table.

ADDR	REGISTER	R/W	7	6	5	4	3	2	1	0	ENABLE
$0007	WATCH DOG	R									
WDT	TIMER STATUS	W								WDT(0)	1 = CLR

Example: Clear Watch-Dog Timer

```
MainPGMLoop:
    JSR     Clear_WDT
    ....                    ;Long program will over
                            ;Watch-Dog Timer
    JSR     Clear_WDT       ;so need call clear WDT
                            ;subroutine again.
    ....
    JMP     MainPGMLoop
Clear_WDT:
    LDA     #01h
    STA     WDT             ;WDT ($0007), clear
                            ;$0007 B0 WDT register.
    RTS
```

4. ILLEGAL ADDRESS RESET (IAR) (see Appendix E)

The internal reset of IAR generated when an instruction opcode fetch occurs from an address not implemented in the RAM ($00C0-$00FF) nor ROM ($0400-$0FFF). The IAR will generate the reset signal that will reset the CPU and other peripherals.

5. LOW VOLTAGE RESET (LVR) (see Appendix E)

The internal LVR reset generated when VDD falls below the specified LVR trigger voltage value (2.2 volt.) at least one CPU clock cycle.

INTERRUPT - see Appendix A, B, F, G (Interrupt Diagram)

1. SOFTWARE INTERRUPT (BRK)

The BRK is an executable instruction interrupt since it executed regardless of the state of the I-bit in the processor status register flag (inside CPU). When BRK occurred, jump to IRQ_routine. As with any instruction, interrupts pending during the previous instruction is served.

2. EXTERNAL INTERRUPT

The External interrupt sources include IRQ pin, PA3 - 0 and PA7. The IRQ pins provide an asynchronous interrupt to the CPU by program control. The PA3-0 can be mask option as an external interrupt. PA7 can be programmed as an external interrupt, not by mask option. The PA7 and IRQ pin are designed with Schmitt Trigger input and low active, but PA3 - 0 are high active.

ADDR	REGISTER	R/W	7	6	5	4	3	2	1	0	ENABLE
$0006	IRQ CONTROL &	R	0(0)	0(0)	0	0	IRQF(0)	IRQF1(0)	IRQE1	IRQE	
IRQS	STATUS	W	IRQR1	IRQR					(0)	(0)	1 = SET

3. IRQ, PA3 - 0 INTERRUPT (see Appendix A, F, G)

The IRQ/PB5 pin can be selected to I/O or I/O with IRQ by program. When IRQ function is selected, the IRQ pin is the main external source of an interrupt with active-low polarity. This pin is connected to a Schmitt trigger input. Since it is an open-drain mode, it needs to be pulled-up externally. When PB5 I/O function is selected, PB5 is normal I/O with open-drain always. When IRQE1 is disabled, the interrupt flag of IRQ, IRQF, will be cleared during creating interrupt. However, if IRQE1 is enabled, the IRQF will not be cleared by interrupt. This interrupt source can be either " Edge-Trigger" or "Level-Trigger". It is selected by mask option. If mask option is set to “Edge-Trigger” mode, the following conditions will cause IRQ interrupt:

1). Falling edge on the IRQ pin.
2). Rising edge on any of PA3 - 0 pin. (If PA3 - 0 is mask option enabled.)

If mask option is set to “Edge-Level Trigger” mode, the following conditions will cause IRQ interrupt:

1). Falling edge and Low level trigger on the IRQ pin.
2). Rising edge and High level on any one of PA3 - 0 pin. (If PA3 - 0 is mask option enabled.)

When IRQ pin or PA3 - 0 pins generate an interrupt (it sets IRQF ($0006 bit3) = 1), the IRQE (if set $0006 bit0 = 1, enable the interrupt function of IRQ) controls whether the interrupt request being sent to CPU. The IRQR ($0006 bit6) is the IRQ pin and PA3 - 0 pins interrupt acknowledge. When IRQR = 1, it will clear the interrupt flag, IRQF.

4. PA7 INTERRUPT (see Appendix B, G)

The PA7 interrupt is falling-edge trigger. It is controlled by IRQE1 ($0006 bit 1). When PA7 interrupt occurred, the interrupt flag of PA7, IRQF1 ($0006 bit2), will be set. The IRQR1 ($0006 bit7) is the PA7 pin interrupt acknowledge. When IRQR1 = ’1’, it will clear the interrupt flag IRQF1 ($0006 bit2 = 0).

Example: Use IRQ pin, PA3 - 0, PA7 as interrupt.

```
            LDA  #%11000011    ;enable IRQ, PA3 - 0,
                               ;PA7 and clear
                               ;interrupt Flag
            STA  IRQS          ;IRQS = $0006
            ....               ;Other working
IRQVacter:  LDA  IRQS          ;Interrupt
                               ;subroutine.
            AND  #%00000100    ;check interrupt of
                               ;PA7
            BNE  PA7_IRQ
PA03_IRQ:   LDA   IRQS
            AND  #%00001000    ;check interrupt of
                               ;PA3 - 0
            BEQ  IRQ_END       ;no PA3 - 0 & PA7
                               ;external interrupt
            ....               ;PA3 - 0 interrupt
                               ;work something.
            LDA  #%01000011    ;set PA3 - 0, PA7 &
                               ;clear PA3 - 0 IRQ
                               ;Flag.  But
            JMP  IRQ_END       ;don't clear PA7 IRQ
                               ;Flag for next IRQ of
                               ;PA7.
```

```
PA7_IRQ:    ....              ;PA7 interrupts
                              ;work something.
            LDA   #%10000011  ;set PA3 - 0, PA7 &
                              ;clear PA7 IRQ Flag,
                              ;but do not clear PA3
                              ;- 0 IRQ Flag for next
                              ;IRQ.
IRQ_END:    STA   IRQS
            RTI
```

Note*: The IRQ pin is not register-mapped; so, it could not acknowledge from register. It needs software check only.

5. TIMER INTERRUPT (TIMER) (see Appendix H)

The timer's interrupt is generated by the multi-function timer when either a timer overflow or a real-time interrupt has occurred. The timer-interrupt flags (TOF, RTIF), enabling bits (TOFE, RTIE) and timer-interrupt-acknowledge bits (TOFR, RTIFR) are all for the timer interrupt in the Timer Control & Status Register (TCS) located at $0004. The I-bit in the Processor Status Flag (inside of CPU) must be cleared to '0' to ensure the interrupt is enabled. For more details on settings of the Timer Control & Status Registrar (TCS), please see the MULTI-FUNCTION TIMER section.

6. MULTI-FUNCTION TIMER- See Appendix H (Timer Block Diagram)

The timer is a 15-bit multi-function ripple Up-Counter. The feature functions include Timer Overflow, Real Time Interrupt (RTI), Power on Reset, and Watch-Dog-Timer Reset (WDT). When the Timer Counter Register (TCR $0005) overflows, the Timer Overflow Flag (TOF) will be set and TOF = 1 will occur an interrupt request to CPU if Timer Overflow Enable is set (TOFE = 1). As long as TOFR = '1', the TOF flag bit is always cleared. The Real Time Interrupt Flag (RTIF) will be set when 1 of 4 selections (RT1, RT0) is active. RTIF = 1 will generate an interrupt request to CPU if Real Time Interrupt Enable set (RTIE = 1). Whenever RTIFR = 1, the RTIF flag bit will be cleared. When a RESET is occurred, RT1 and RT0 of TCS are set as '1' and rest of the bits on TCS are set as '0'.

7. TIMER REGISTER

The 15-Stage timers contain two registers: Timer Counter & Timer Control/Status Register.

■ TIMER COUNTER REGISTER (TCR) - $0005

The timer counter register is a read-only register that contains the current value of the 8-bit at the beginning of the timer chain. The value of each bit of the TCR is shown in following table. The register is cleared by reset.

ADDR	REGISTER	R/W	7	6	5	4	3	2	1	0	ENABLE
$0005	TIMER COUNTER	R	TMR7(0)	TMR6(0)	TMR5(0)	TMR4(0)	TMR3(0)	TMR2(0)	TMR1(0)	TMR0(0)	
TCR	REGISTER	W									

Timer Counter Register (TCR)

■ TIMER CONTROL/STATUS REGISTER (TCS)- $0004

The TCS contains the timer interrupt flag (TOF, RTIF), the timer interrupt enable (TOFE, RTIE), timer interrupt acknowledge (TOFR, RTIFR) and real timer interrupt rate select bits (RT1, RT0). Bit 2 and bit 3 are write-only bits that will read as logical zeros. The following table shows the value of each bit in the TCS, which is set to 0. RT1 and RT0 are set to 1 by reset initially.

ADDR	REGISTER	R/W	7	6	5	4	3	2	1	0	ENABLE
$0004	TIMER CONTROL	R	TOF(0)	RTIF(0)	TOFE	RTIE	0(0)	0(0)	RT1	RT0	
TCS	& STATUS	W			(0)	(0)	TOFR	RTIFR	(1)	(1)	1 = SET

Timer Control/Status Register (TCS)

8. TOF - Timer Overflow Flag (The TOF is a read-only flag bit.)

1 = Set when the 8-bit ripple counter rolls over from $FF change to $00. A timer interrupt request will generate if TOFE also set.

0 = Reset by writing a logical one to the TOF acknowledgment bit, TOFR.

9. RTIF - Real Time Interrupt Flag (The RTIF is a read-only flag bit.)

1 = Set when the output of the chosen Real Time Interrupt stage goes active. A timer interrupt request will generate if RTIE is set.

0 = Reset by writing a logical one to the RTIF acknowledges bit, RTIFR.

10. TOFE - Timer Overflow Enable

The TOFE is an enable bit that allows generation of timer interrupt upon overflow of the Timer Counter Register.

1 = When set, the timers interrupt generated when the TOF flag bit set.

0 = When cleared, there is no timer interrupt being generated for TOF1 flag.

11. RTIE - Real Time Interrupt Enable

The RTIE is an enable bit that allows generation of a timer interrupt by the RTIF bit.

1 = When set, the timer interrupt generated when the RTIF flag bit set.

0 = When cleared, there is no timer interrupt being generated even though RTIF flag is set.

12. TOFR - Timer Overflow Acknowledge

The TOFR is an acknowledgment bit that resets TOF flag. Reading the TOFR will always return a logical zero.

1 = Clears the TOF flag bit.

0 = Does not clear the TOF flag bit.

13. RT1:RT0 - Real Time Interrupt Rate Select

The RT0 & RT1 control bits select one of four taps for the Real Time Interrupt circuit. The following table shows the available interrupt rates for two frequency values of timer 1 clock selected by mask option.

Example: CPU Clock f_{CPU} = 1.0MHz (Oscillation Frequency = 2MHz) with two options for Timer 1 clock

	RTI RATES			MIN. WDT RESET (=RTI/8)		
RT1:RT0	Divider	option $f_{CPU}/4$	option $f_{CPU}/1$	Divider	option $f_{CPU}/4$	option $f_{CPU}/1$
00	2048	8.192ms	2.048ms	16384	65.536ms	16.384ms
01	4096	16.384ms	4.096ms	32768	131ms	32.768ms
10	8192	32.768ms	8.192ms	65536	262ms	66ms
11	16384	65.536ms	16.384ms	131072	524ms	131ms

(RT1, RT0) & WDT Interrupt Frequency Table at f_{CPU} = 1.0MHz.

Example: Enable Timer Counter & RTI (RT1 = 1,RT0 = 0), use 2.0MHz Rosc.

```
    LDA  #%00111110    ;TCS $0004 set TOFE,
                       ;RTIE, RT1, RT0 = 10,
    STA  TCS           ;& clear interrupt
                       ;Flag
    ....               ;Other instruction
                       ;for initialized or
                       ;work
    CLI                ;software enable
                       ;interrupt
```

```
IRQ_Vacter: LDA  TCS           ;Interrupt
                               ;subroutine.
            AND  #%10000000    ;check Timer Overflow
                               ;interrupt
            BNE TO_IRQ
RTI_IRQ:    LDA TCS
            AND #%01000000     ;check Real Time
                               ;Interrupt
            BEQ IRQ_END
            ....               ;Working for used
                               ;RTI
```

```
            LDA  #%00110110    ;set RTI, TO enable
                               ;again, only clear
                               ;RTIF
            JMP IRQ_END
TO_IRQ:     ....               ;Working for used
                               ;Timer Overflow (TO)
            LDA #%00111010     ;set RTI, TO enable
                               ;again, only clear
                               ;TOF
IRQ_END:    STA      TCS
            RTI
```

WAIT / STOP MODE

The WAIT mode function will set CPU clock disabled and Timer counter enabled if WAIT $0008 bit0 = 1. The TOF, RTI, or external interrupt will make CPU being recovered normally from wait mode interrupt point next address. The STOP mode function will set CPU and Timer counter disabled if STOP $0008 bit4 = 1 and only the external interrupt will make CPU and Timer counter being recovered normally from Stop mod interrupt point next address.

ADDR	REGISTER	R/W	7	6	5	4	3	2	1	0	ENABLE
$0008	STOP & WAIT	R									
SNW		W				STOP(0)				WAIT(0)	1 = SET

Example:

```
            ....               ; Normal working.
Wait_Set:   LDA  #%00000001    ;STPWAT $0008, set
                               ;Wait modes enable.
            STA  STPWAT        ; enter the WAIT mode.
            NOP                ;*
            NOP                ;
            ....               ;Normal working.
            JMP  MainPGMLoop
```

```
Stop_Set:   LDA  #%00010000    ;set Stop mode
                               ;enable.
            STA  STPWAT        ; enter the STOP mode.
            NOP                ;*
            NOP                ;
            ....               ;Normal working.
            JMP  MainPGMLoop
```

Note*: To add two more NOPs to ensure proper wake up is preferred.

ABSOLUTE MAXIMUM RATING

Power Supply Voltage	VCC = +2.4V to + 5.5V
Input Voltage	V_{IN} = - 0.3V to VCC+0.3V
Output Voltage	V_{OUT} = 0V to VCC
CPU clock	From 200KHz to 6.0MHz
Operating Ambient Temperature	T_{OPR} = - 0°C to +70°C
Storage Temperature	T_{STR} = -20°C to +70°C

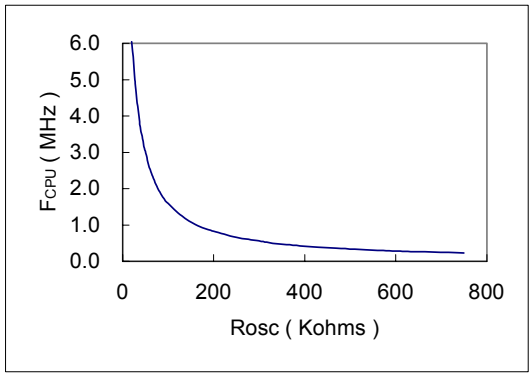
Note: Stresses beyond those given in the Absolute Maximum Ratings table may cause operational errors or damage to the device. For normal operation conditions see AC/DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, VCC = 5V)

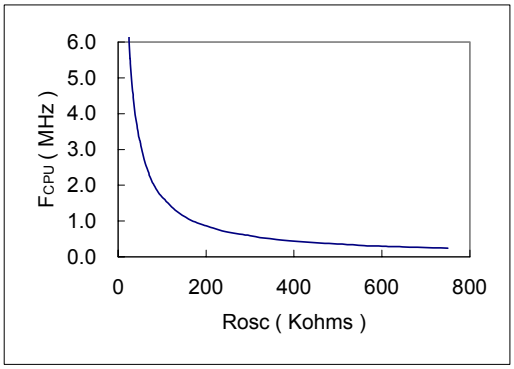
Characteristic	Condition	Symbol	Min.	Typ.	Max.	Unit
Output high voltage PA5 - 0*, PB0*	I_{OH} = -8mA	V_{OH}	2.4	-	-	V
Output low voltage PA7 - 0, PB0	I_{OL} = 8mA	V_{OL}	-	-	0.4	V
Output low voltage PB1	I_{OL} = 25mA	V_{OL}	-	-	0.5	V
Input high voltage PA5 - 0, PB1 - 0		V_{IH}	3.5	-	-	V
Input low voltage PA5 - 0, PB1 - 0		V_{IL}	-	-	1.4	V
Positive Going input threshold voltage PA6, PA7, IRQ/PB4, RESET/PB5		V_{IH}	-	2.0	-	V
Negative-going input threshold voltage PA6, PA7, IRQ/PB4, RESET/PB5		V_{IL}	-	0.8	-	V
I/O port Hi-Z leakage PA5 - 0, PB1 - 0	Pull-Down/up inactive	I_{IZ}	-	-	10	μA
Pull-down resistance PA5 - 0, PB0	V_{IN} = 5V	R_{PUDWN}	-	100	-	KΩ
Pull-up resistance PA6, PA7	Pull-up always V_{IN} = 0V	R_{PULLUP}	-	5.0	-	KΩ
Pull-up resistance PB1	V_{IN} = 0V	R_{PULLUP}	-	100	-	KΩ
Power consumption		I_{CC}	-	2.0	-	mA
Stand by current		I_{STB}	-	5.0	-	μA
LVR trigger voltage		V_{LVR}	-	2.2	-	V

THE RELATIONSHIP BETWEEN THE R_{OSC} AND THE F_{OSC}

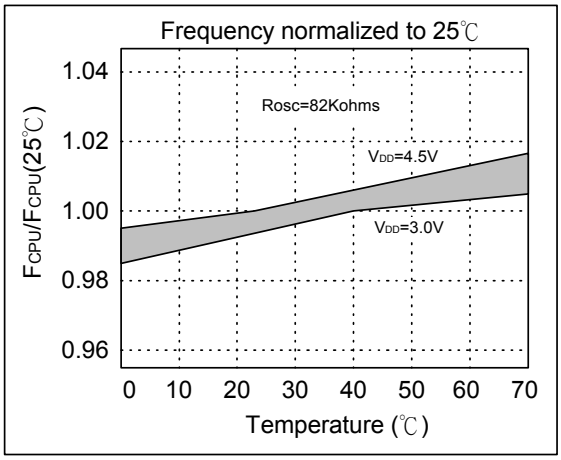
1. VDD = 3V , T_A = 25℃



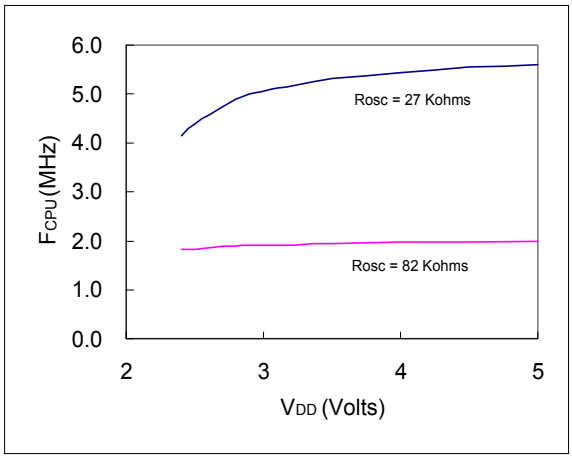
2. VDD = 5V , T_A = 25℃



3. FREQUENCY vs. TEMPERATURE



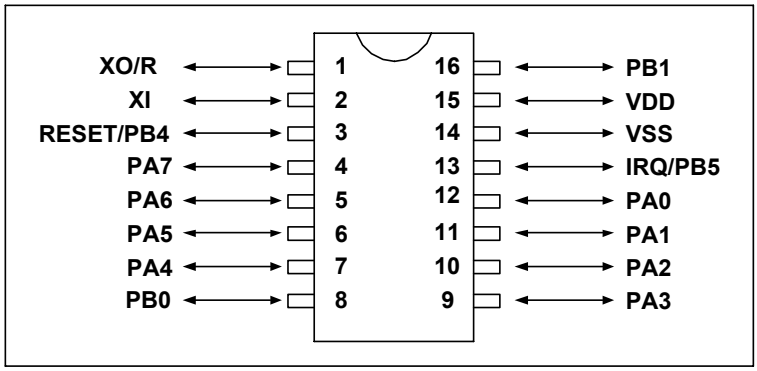
4. FREQUENCY vs. VDD



PIN DESCRIPTION

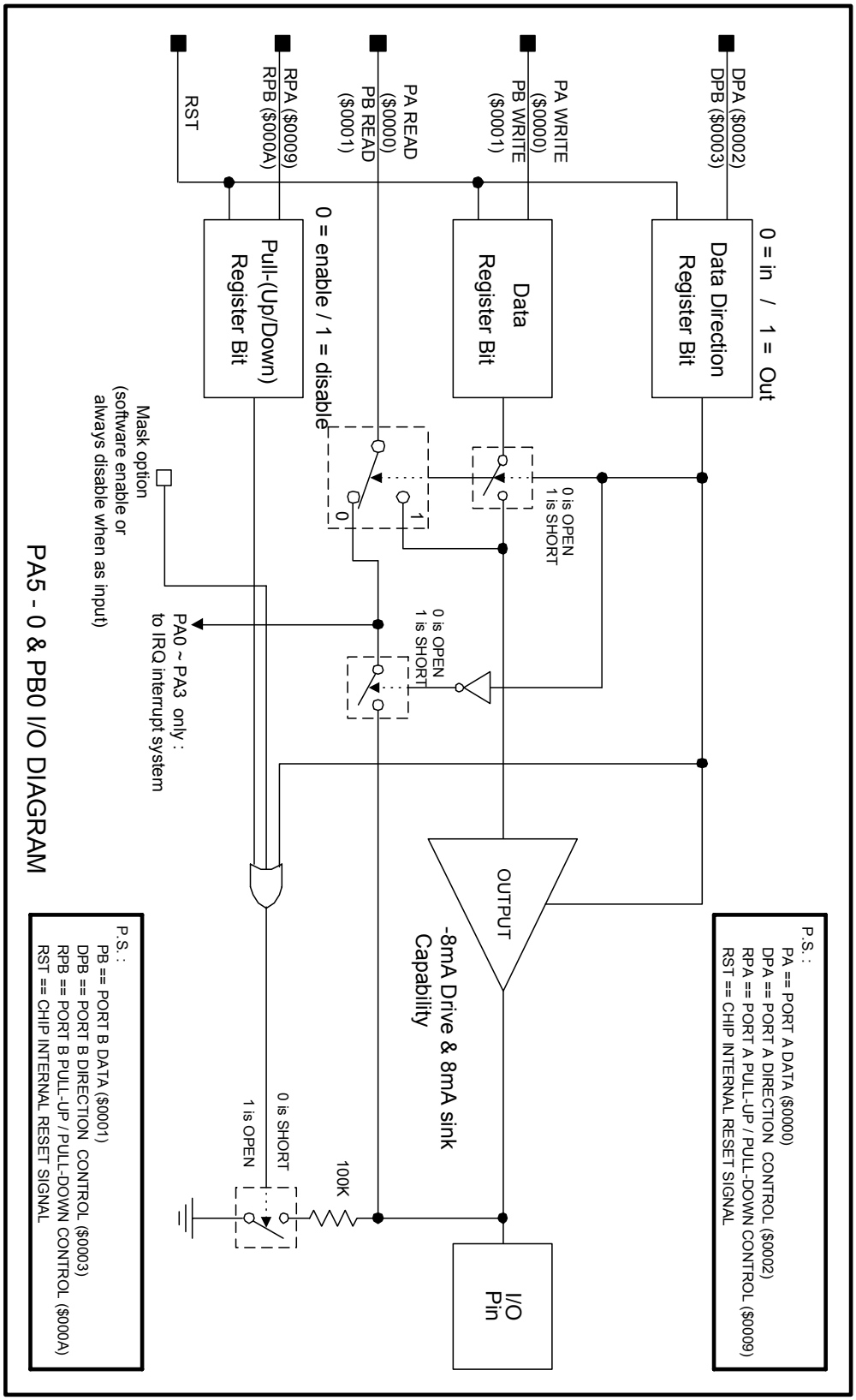
Mnemonic	PIN No.	Type	Description
VDD	15	I	Power
VSS	14	I	Ground
XO/R	1	I	Crystal in or resistor
XI	2	O	Crystal out or Ext. Clock in
RESET/PB4	3	I/O	External reset or PB4 (I/O)
IRQ/PB5	13	I/O	Interrupt in or PB5 (I/O)
PA3 - 0 PA7 - 4	12 - 9 7 - 4	I/O	Port A
PB0 PB1	8 16	I/O	Port B

PIN ASSIGNMENT

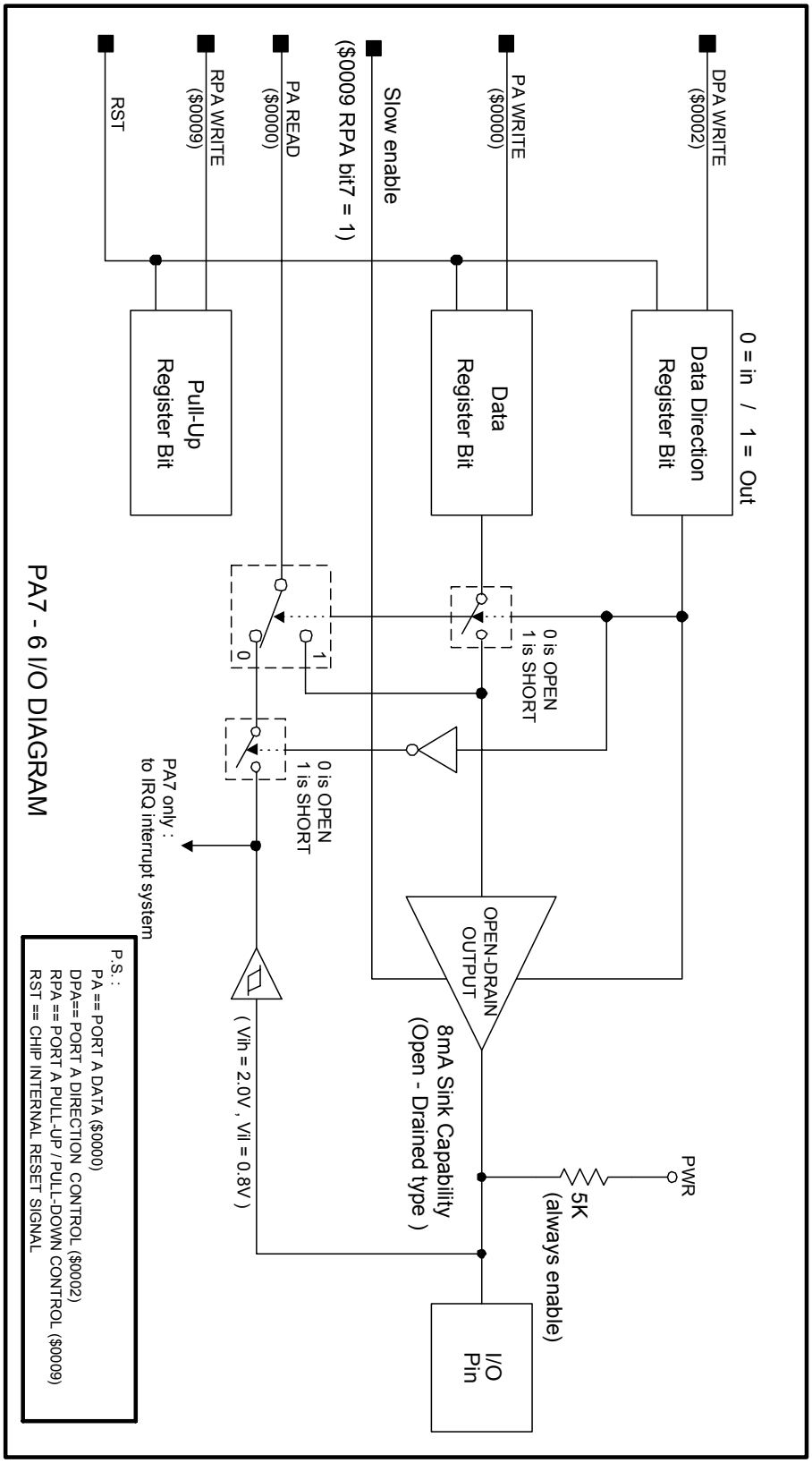


16 PIN DIP PACKAGE

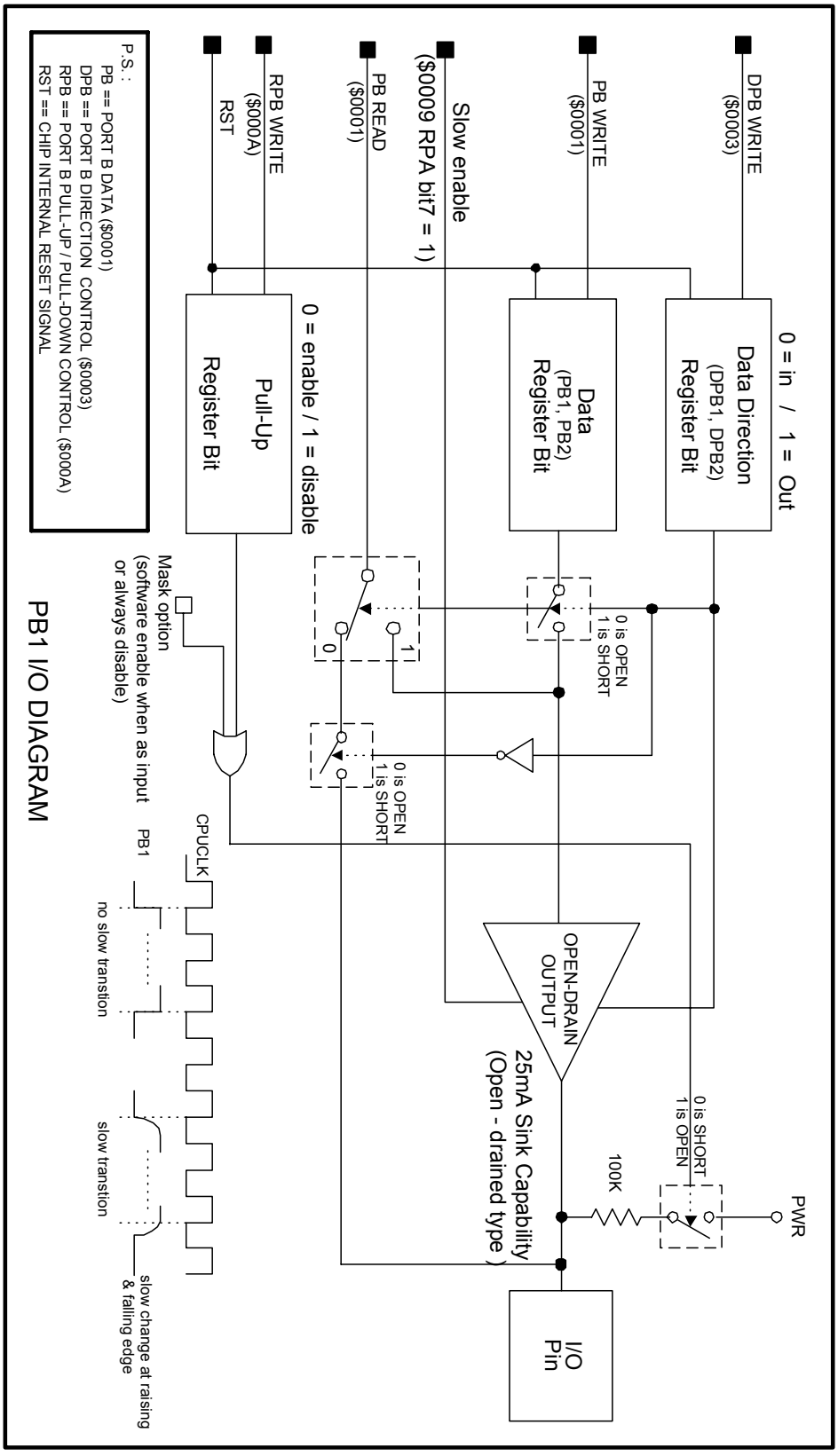
APPENDIX A: PA5 - 0 & PB0 I/O DIAGRAM



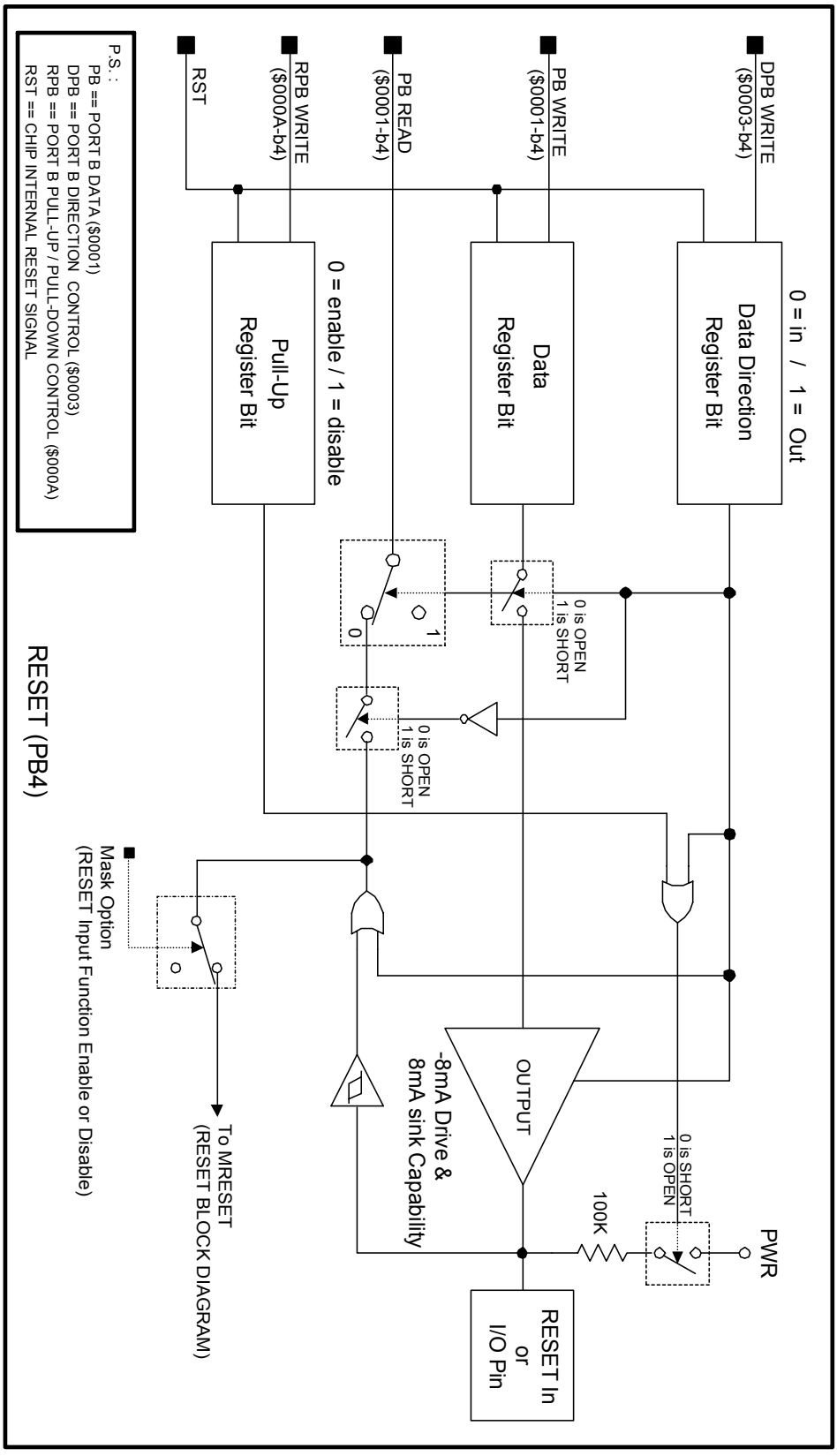
APPENDIX B: PA6, PA7 I/O DIAGRAM



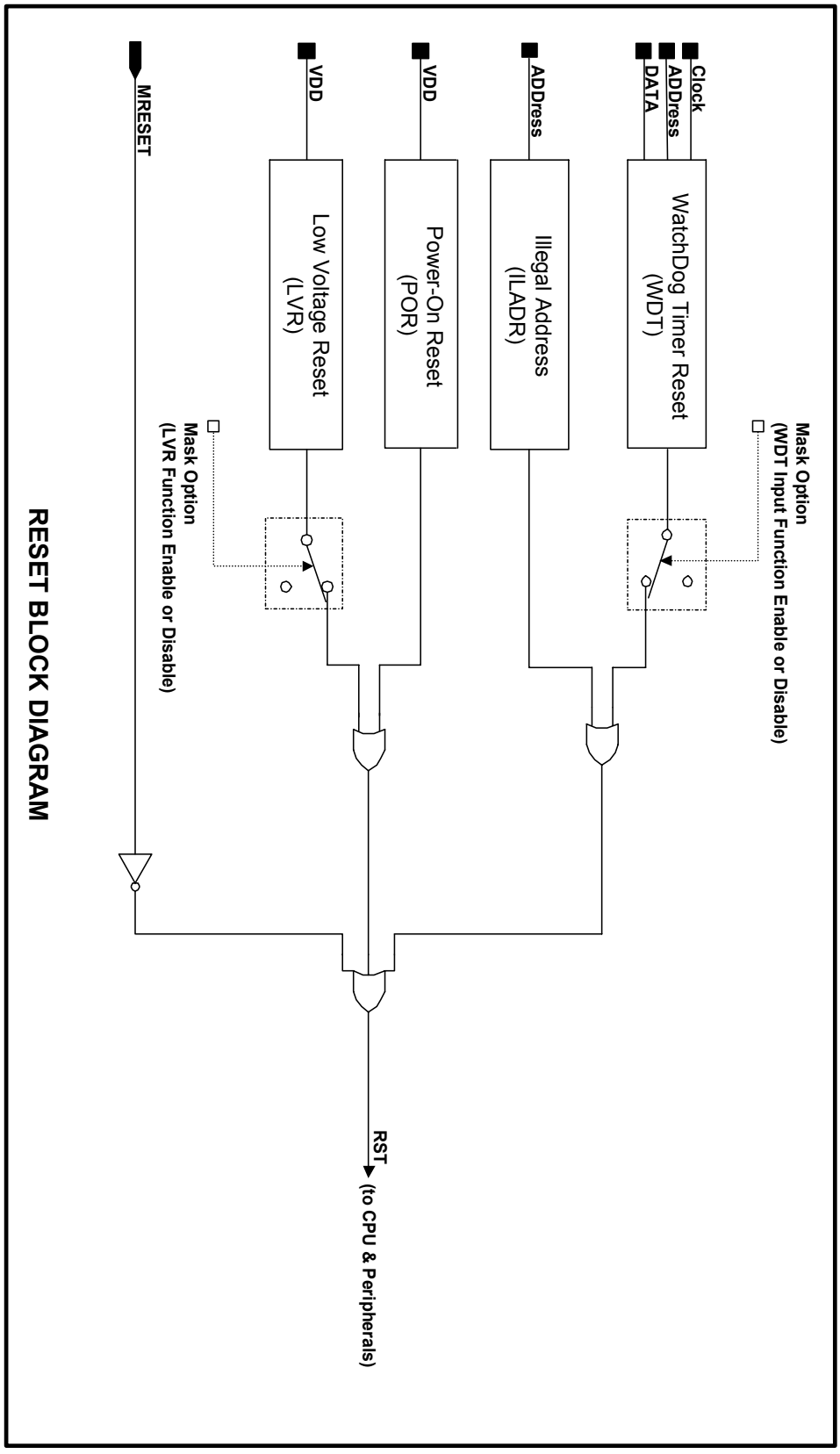
APPENDIX C: PB1 I/O DIAGRAM



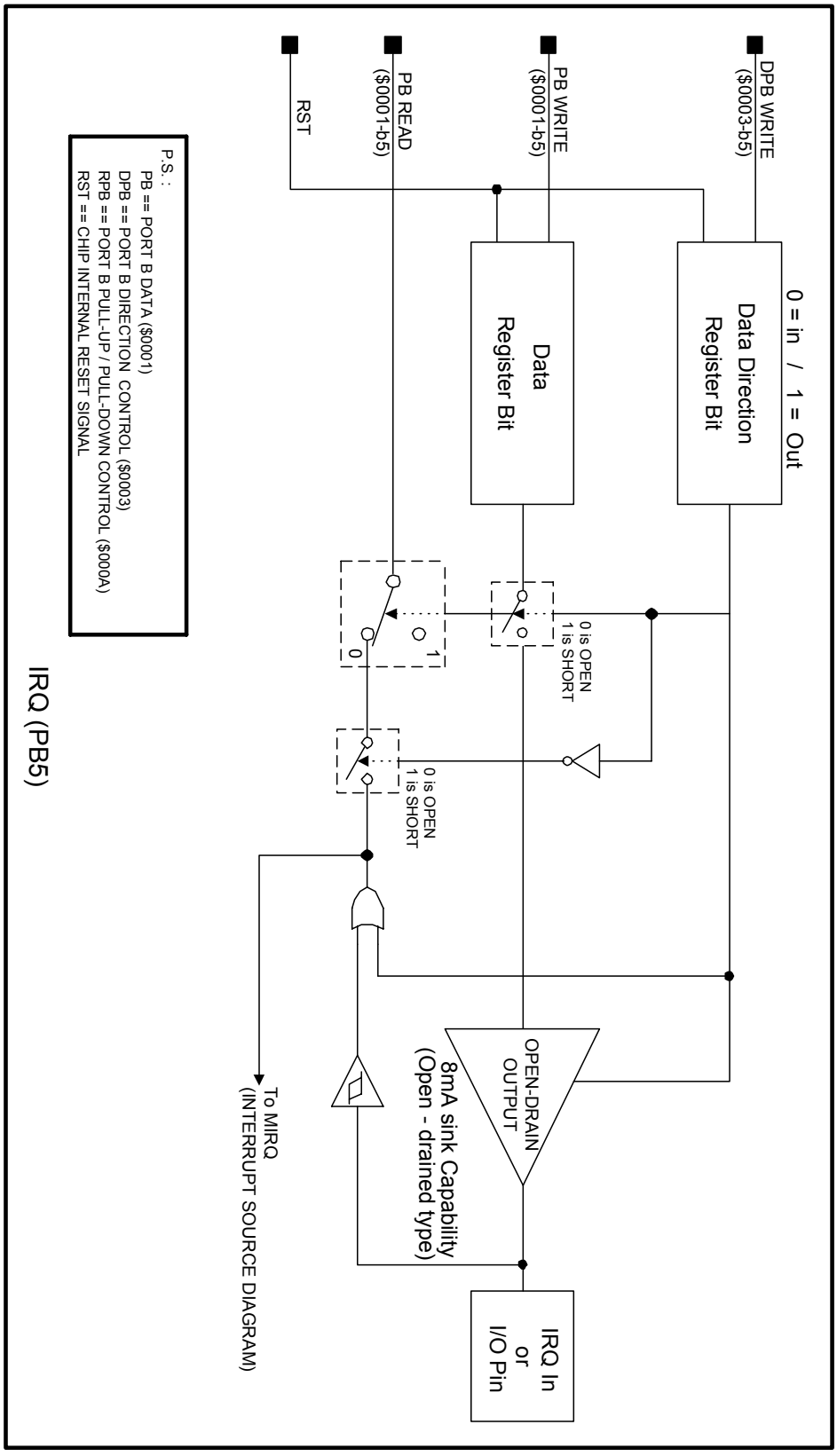
APPENDIX D: PB4 & RESET I/O DIAGRAM



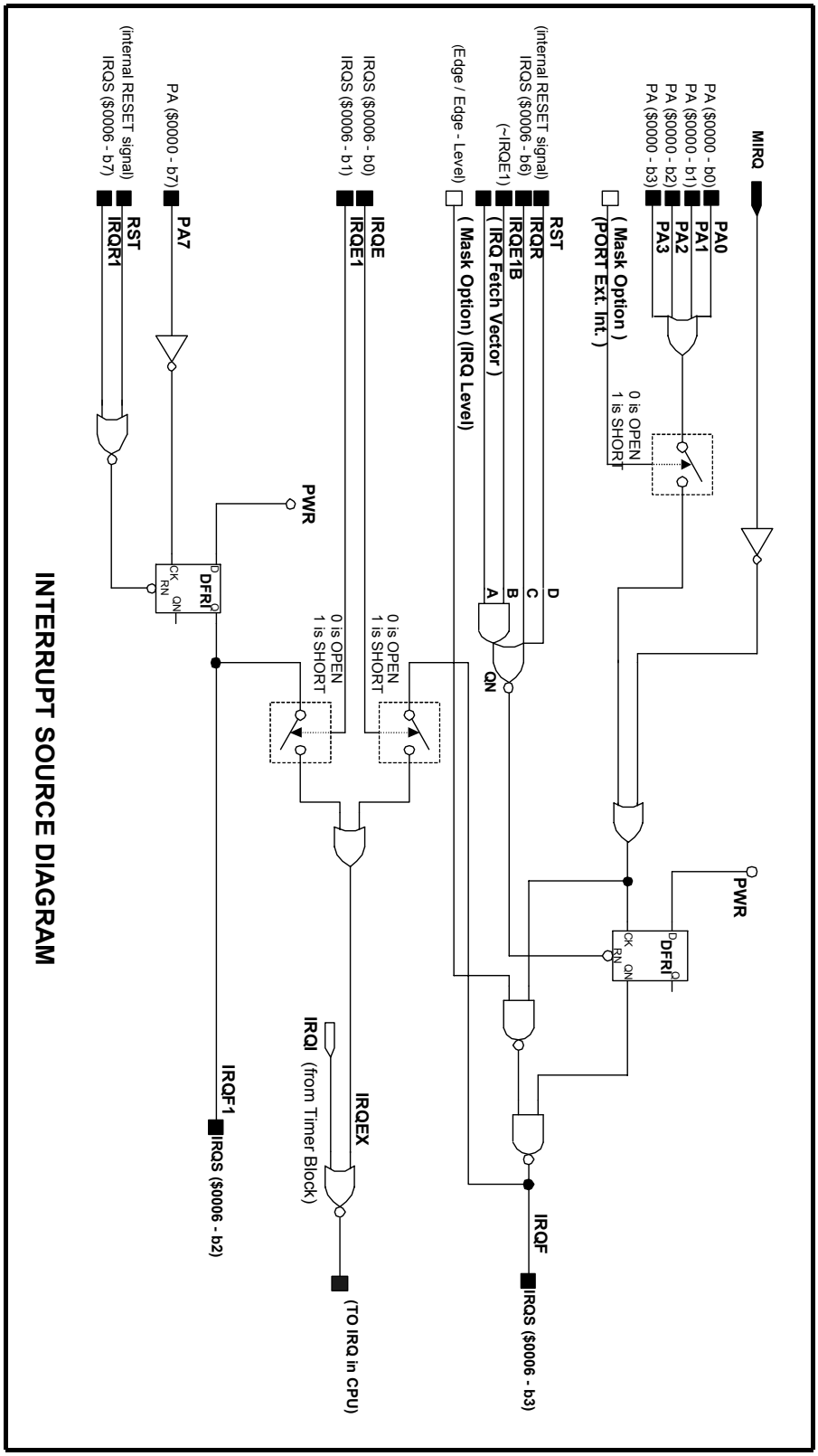
APPENDIX E: RESET BLOCK DIAGRAM



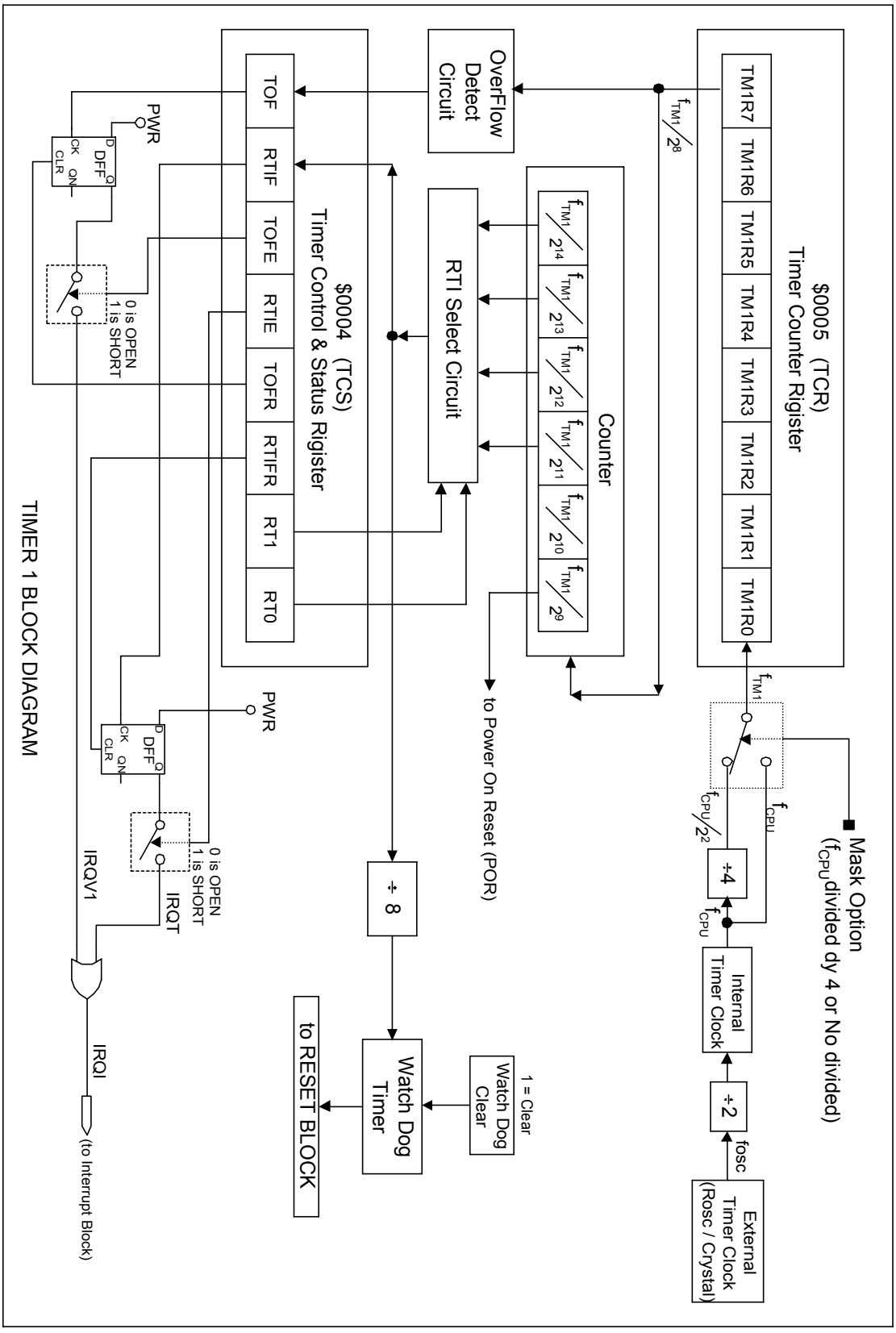
APPENDIX F: PB5 & IRQ I/O DIAGRAM



APPENDIX G: INTERRUPT SOURCE DIAGRAM

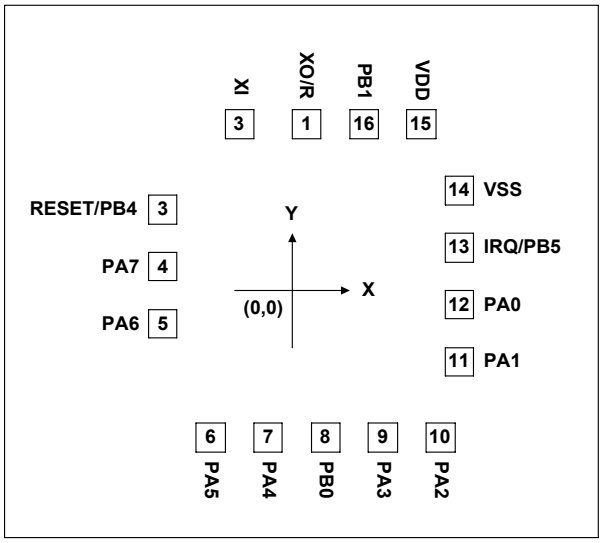


APPENDIX H: TIMER BLOCK DIAGRAM



APPENDIX I: PAD ASSIGNMENT AND LOCATIONS

1. PAD ASSIGNMENT



Chip Size: 1520μm x 1560μm

The IC substrate should be connected to VSS

Note: 0.1μF capacitor between VDD and VSS should be placed to IC as close as passible.

2. PAD LOCATIONS

Pad No	Pad Name	X	Y
1	XO	51	609
2	XI	-166	610
3	RESET / PB4	-574	191
4	PA7	-574	-26
5	PA6	-574	-375
6	PA5	-342	-610
7	PA4	-126	-610
8	PB0	91	-610
9	PA3	307	-610
10	PA2	523	-610
11	PA1	590	-288
12	PA0	590	-72
13	IRQ / PB5	590	186
14	VSS	590	365
15	VDD	539	609
16	PB1	283	610

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REVISION HISTORY

Date	Revision #	Description	Page
NOV. 04, 1997	0.1	Original	
SEP. 17, 1997	0.2	1. Modify "*BLOCK DIAGRAM*" 2. Modify grammar	
JAN. 09, 1998	0.3	1. Add Operation Voltage Range: 2.4V - 6.0V in "*FEATURES*" and "*DC ELECTRICAL CHARACTERISTICS"* 2. Chang font: "Arial" 3. Add "*EMULATION BOARD*" and "*PIGGY BACK BOARD*" User Guide	
MAR. 02, 1998	1.0	Delete "*PRELIMINARY*"	
JUN. 04, 1998	1.1	1. Add "*FREQUENCY vs. VDD, TEMPERATURE*" 2. Revise the pin naming in "*BLOCK DIAGRAM*", "*PIN ASSIGMENT*", "*BONDING DIAGRAM*", "*BONDING CORRDINATE*": OSC2 -> XO, OSC1 -> XI	
DEC. 13, 1999	1.2	1. Add PIN No. in "*PIN ASSIGNMENT*" 2. Add "*DISCLAIMER*" 3. Renew to a new document format	
NOV. 07, 2000	1.3	1. Wording improvement 2. To revise the CPU low bound clock range from 1KHz to 200KHz 3. To correct the I/O block diagrams on Appendix C: PB1 I/O Diagram, Appendix F: PB5 & IRQ I/O Diagram, and Appendix G: Interrupt Source Diagram 4. To remove Appendix D: I-V Curve of PB1, and Appendix L: Piggyback Board 5. Add "Note: The 0.1uF capacitor between VDD and VSS…" 6. Add "*REVISION HISTORY*" 7. Renew to a new document format	23 26